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Date of Deposit April 15, 2002  
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April 12, 2002

## VIA EXPRESS MAIL LABEL NO. EI783896998US

Box Patent Application  
Commissioner for Patents  
Washington, D.C. 20231

Re:	Applicant:	Infineon Technologies, AG
	Serial No:	10/069806
	English Title:	Driver circuit and method for operating a driver circuit
	Attorney Docket No:	32226.18

Dear Sir:

Enclosed for filing please find the following:

1. Preliminary Amendment; and
2. A self-addressed stamped post card to return to us acknowledging receipt of the enclosed document.

It is my understanding that there is no fee required for this filing. If that understanding is incorrect, the Commissioner is hereby authorized to charge any payment of the required fees to Deposit Account No. 02-3732. This filing is associated with Briggs and Morgan's customer number 32300.

Very truly yours,

Jeffrey R. Stone

JRS/maf  
Enclosures

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#9  
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Amend  
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atg

Re: U.S. Patent Application 10/069806 ) PATENT  
)  
)  
German Title: Treiberschaltung und Verfahren zum )  
Betreiben einer Treiberschaltung )  
)  
)  
English Translation: Driver circuit and method for operating )  
a driver circuit )  
)  
)  
Applicant: Infineon Technologies, AG )  
)  
)  
Inventors: Christian Paulus )  
Ralf Klein )  
)  
)  
Attorney Docket No: 32226.18 )

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SEP 25 2002

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Honorable Commissioner of Patents and Trademarks  
Washington, D.C. 20231

Sir:

**PRELIMINARY AMENDMENT**

In the above-entitled patent application, please amend the application as follows:

In the Claims

- a' SUB B6 1. (amended) A driver circuit, having at least one input node for an input signal and  
2 at least one output node for an output signal, having one or more, preferably two, sub-drivers and  
3 having a feedback circuit, which has one or more evaluation circuits and one or more feedback  
4 capacitors, the evaluation circuit(s) being connected to the sub-driver(s) and the feedback  
5 capacitor(s) respectively being provided between an output node of the driver circuit and an  
6 input node of an evaluation circuit, the at least one evaluation circuit having a first inverter stage,  
7 coupled to the input node of the evaluation circuit, and also a second inverter stage, connected in  
8 series with the first inverter stage, the first inverter stage being short-circuited with the input  
9 node.